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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/954,596	09/12/2001	Anton Gunzinger	FREI P033US-2	8857

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EXAMINER	
ELLIS, RICHARD L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/954,596	GUNZINGER, ANTON	
	Examiner	Art Unit	
	Richard Ellis	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/11/2005 & 7/5/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-31,33 and 34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-31,33 and 34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 16-31 and 33-34 remain for examination.

2. The text of those sections of Title 35, US Code not included in this action can be found in a prior Office Action.

3. The following in a quotation of the first paragraph of 35 USC 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 16-31 and 33-34 are rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. This is a written description rejection.

Applicant's arguments in the reply filed July 5, 2005, being directed only to the disputed definition of the claim term "message-passing communications network", indicate that applicant clearly believes that his novelty over the applied Parrish et al. reference resides in the details of this particular "message-passing communications network". However, applicant's specification provides absolutely no written description describing this supposed special novel "message-passing communications network" that applicant believes differentiates the claims from the applied Parrish et al. reference. In fact, applicant's arguments admit that the term "message-passing" is never defined by the specification:

> "It is correct that the term "message passing" is not defined in the specification or claims" (pg. 9 of response of July 5, 2005)

Additionally, as was shown in the last office action (pg. 4, paper number 20050503), the term "message-passing communications network' was never used in the specification. Furthermore, the specification explicitly states that the type of network utilized is immaterial to the invention:

> "These at least two processor elements are connected to one another by a shared communications network O appropriately evincing wide bandwidth and low latency. **No assumptions are made concerning the communications network.** Illustratively "Fast Ethernet", ATM, GigaBit Ethernet, Fiber Channel or any other fast network may

be used." (emphasis added) (specification, pg. 4, lines 6-9)

As is clearly evidenced by this portion of the specification, applicant's invention when filed did not hinge upon any supposed novelty of the particular network utilized to interconnect the processor elements. Accordingly, because when filed applicant clearly felt the novelty did not reside in the network, applicant did not further describe the network in any further detail. Therefore, if now, novelty does reside in some special secret network architecture as argued by applicant, then applicant's specification clearly did not provide any written description to indicate to one of skill in the art what special secret network architecture applicant has possession of at the time of filing the application.

5. Claims 16-31 and 33-34 are rejected under 35 USC 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. As detailed above in the written description rejection of applicant's claims, not only is the specification silent as to any details of the particulars of the "message-passing communications network" of the invention, it specifically indicates that the particulars of the "message-passing communications network" are immaterial to the invention. Accordingly, if as argued by applicant now the novelty resides in some special secret particular of the "message-passing communications network", the specification can not possibly have enabled one of skill in the art to make and/or use the invention because it is totally silent as to any novel details regarding the "message-passing communications network". Therefore, the specification fails to provide enablement to allow one of skill in the art to build this special secret "message-passing communications network" that applicant's arguments assert provides novelty over the Parrish et al. reference.

6. Claims 16-31 and 33-34 are rejected under 35 USC 112, first paragraph, because the best mode contemplated by the inventor has not been disclosed. Evidence of concealment of the best mode is based upon applicant's arguments in the appeal brief filed March 22, 2005 (paper number 20050322) in combination with the arguments filed in the reply received July 5,

2005 (paper number 20050705). Applicant's arguments in the brief, as detailed in the examiner's answer (paper number 20050503, mailed May 3, 2005, herein incorporated by reference) clearly show that applicant believes that his novelty over the Parrish et al. reference resides in part and/or in whole in unstated, special, secret, details of the claimed "message-passing communications network". If in fact applicant's novelty resides in these secret unstated details about the "message-passing communications network", then by failing to present any of those details in the specification (see above rejections for written description and enablement, and see the examiner's answer for a thorough treatment) applicant has concealed the best mode contemplated by the inventor. I.e., if the novelty of the invention resides in the "message-passing communications network" as argued by applicant, then when the specification is silent as to any details of that "message-passing communications network", the inventor has clearly concealed the best mode.

7. Claims 16-31 and 33-34 are rejected under 35 USC 102(b) as being clearly anticipated by Parrish et al., U.S. Patent 5,117,350. The specification of co-pending application 07/232,155 was incorporated by reference into Parrish et al.'s specification at col. 4 lines 3-8. Definitions from "Yahoo! Education", *The Dictionary of Computers, Information Processing & Telecommunications*, second edition, *Modern Dictionary of Electronics*, and *Microsoft Press Computer Dictionary*, second edition were cited as extrinsic evidence to applicant in paper number 20040913, mailed September 21, 2004. Pages 563-567 and 579 of *Computer Architecture, A Quantitative Approach*, second edition, by David A. Patterson and John L. Hennessy (1996, Morgan Kaufman Publishers) is further cited to further show support for the examiner's position.

Parrish et al., the specification of copending application 07/232,155, and the above three dictionary definitions were utilized to reject applicant's claims in paper number 20050503, mailed May 3, 2005.

8. The rejections are respectfully maintained and incorporated by reference as set forth in the last office action, paper number 20050503, mailed May 3, 2005.

9. Applicant's arguments filed July 5, 2005, paper number 20050705, have been fully considered but they are not deemed to be persuasive.

10. In the remarks applicant argues across pages 1-6 various details that relate to appeal procedure. As this application is no longer at appeal, due to applicant's having filed a Request for Continued Examination on October 11, 2005, those arguments related to appeal procedure are considered moot and will not be further treated.

11. In the remarks, applicant argues in substance:

A. That: "One skilled in the relevant art would know what "message-passing communications network" means. One of the widely known standard textbooks in the field of computer architecture, which includes a chapter on parallel computing, has been *Computer Architecture - A Quantitative Approach* by Patterson and Hennessy ... A true and correct copy of page 640 of this textbook is attached as Exhibit A ... This page distinguishes between "shared memory" parallel processing systems, and "message-passing" parallel processing systems. See for example the underlined sentence in this Exhibit.

With each of these organizations for the address space, there is an associated communication mechanism. For a machine with a shared address space, that address space can be used to communicate data implicitly via load and store operations; hence the name *shared memory* for such machines. For a machine with multiple address spaces, communication of data is done by expressly passing messages among the processors. Therefore, these machines are often called *message passing machines*. (emphasis added)."

This is not found persuasive because applicant's cited section of Patterson et al. simply indicates that machines that communicate by passing messages are called "message passing machines". However, applicant is reminded that the claim term at issue is "message-passing communications network", not "message passing machines", i.e., applicant is claiming a type of network named "message-passing communications network" and arguing that this special type of network is different from that disclosed by Parrish et al. However, this cited section of Patterson et al. provides no further illumination as to what special, secret, architecture applicant believes constitutes the claimed "message-passing communications network" as that term is utilized in the claims and as applicant is arguing differentate the claims from the Parrish et al. reference.

B. That: "The article by Gordon Bell (Exhibit B) likewise reviews the taxonomy (naming terminology) used to distinguish between shared-memory systems and message-passing

systems, particularly at page 37. This article is dated 1992."

This is not found persuasive for the same reasons given above in regards to the Patterson et al. citation. The claim term at issue is "message-passing communications network" and pg. 37 of the Bell document at best indicates a definition for "message-passing" or "message-passing computation", but provides no illumination as to what special secret meaning applicant's intend for their claim term "message-passing communications network".

C. That: "Briefly, the Parrish system concerns processors on a common bus. Buses are not message-passing networks but work in a more direct manner by working directly in a write and read (or 'load' and 'store') manner."

This is not found persuasive because applicant's own exhibits prove that applicant is absolutely incorrect in the above assertion. Applicant's attention is drawn to his own Exhibit B by Gordon Bell, specifically to page 37, the very page that applicant has cited. Applicant's attention is drawn to the lower half of the figure on the page, specifically the "Multicomputers" node where Bell indicates that "Multicomputers" are "Message-Passing". Applicant's attention is further drawn to the line connecting "Multicomputers" to the "Distributed multicomputers (scalable)" node. The fourth and fifth entries of network types connected to the "Distributed multicomputers (scalable)" node state:

> "Fast LANs for high availability and high capacity clusters DEC, Tandem"
> "LANs for distributed processing workstations, PCs"

Applicant's attention is drawn to the fact that both of these sections recite "LAN" which is short for Local Area Network, and that Bell clearly groups both "LAN" nodes beneath the "Message-Passing" node labeled "Multicomputers". Applicant's attention is now drawn the additional cited pages of the Patterson et al. textbook, a textbook that applicant himself has cited. Page 564 of Patterson et al. defines "LAN" as:

> "Local area network (LAN) - This device connects hundreds of computers, and the distance is upto a few kilometers. ..."

Patterson et al. further indicates on pg. 563 that a LAN is one species of the genus "interconnection network". Applicant's attention is now drawn to pg. 579 of Patterson et al. where Patterson et al. describes in his words "The most popular LAN":

> "The most popular LAN, Ethernet, ***is simply a bus*** that can be shared by hundreds of computers.
> Given that the medium is shared, there must be a mechanism to coordinate the use of the shared medium so that only one ***message*** is sent at a time. ..."

The point presented by pg. 579 of Patterson et al. is unmistakable. The most popular LAN (Local Area **Network**), Ethernet, is **simply** a **bus**. And furthermore, that simple **bus** transfers **messages**. Therefore, these mere 46 words written by Patterson et al. totally refute applicant's assertion that a "bus" is not a "message-passing network". Patterson et al. clearly indicates that the most popular **network**, a network that transmits **messages**, is ***simply a bus***. Accordingly, because the worlds most popular message passing network is **simply a bus**, applicant's assertion can be seen as nothing more than completely and wholly incorrect.

D. That: "According to the claimed invention, however, processors are coupled by a message-passing communications network." [as opposed to a bus]

This is not found persuasive because pg. 4 of the specification at line 8 clearly indicate that two networks contemplated by the inventor for use in the invention are "Fast Ethernet" and "GigaBit Ethernet". As was clearly shown above, Ethernet, the most popular LAN (Local Area Network) is ***simply a bus***. Not only that, but Ethernet also transmits **messages** as shown above. Therefore, in two of the inventors own suggested networks for use in interconnecting the processors of his invention, the processors are coupled by ***simply a bus*** that transmits **messages**. As was clearly pointed out in the examiner's answer, Parrish et al. details a bus that has the ability to pass messages. Accordingly, Parrish et al.'s bus is a "message-passing communications network" just as much as "Fast Ethernet" or "GigaBit Ethernet" (as suggested by the inventor) are also "message-passing communications network[s]" even though they too are simply ***busses*** as indicated by Patterson et al..

E. That: "Stating the above in a different way, a shared memory parallel programming system as the one disclosed in the Parrish references can not be at the same time a message passing system, since "message passing" is defined as an alternative to "shared memory."

This is not found persuasive because this passage appears to indicate applicant's confusion as to the Parrish et al. reference. Applicant appears to be improperly and

incorrectly classifying Parrish et al. as a shared memory multiprocessor system, while ignoring the fact that Parrish et al. is in fact not a shared memory multiprocessor system. Applicant's attention is drawn first to the title of the Parrish et al. reference: "Memory address mechanism in a ***distributed memory architecture***". The very title of the Parrish et al. reference clearly indicates that the Parrish et al. system fits into the node "Distributed multicomputers" of pg. 37 of applicant's own Bell publication citation. Applicant's attention is then drawn to the immediate fact that the "Distributed multicomputers" node is classified underneath the "message-passing" node. Therefore, applicant's own citation of Bell refutes applicant's assertion about the Parrish et al. reference. Further evidence of the fact that the Parrish et al. system fits within the "Distributed multicomputers" node of pg. 37 of the Bell publication can be found at col. 8 lines 13-19 where Parrish et al. states:

> "Each node includes an ***industry standard digital computer*** (ISC) 113, 133 having its own private memory, identified as IPM in the memory table in the figure, that is connected to a local memory 114 134 via a VME bus 115, 135 and a VSB bus 116, 136, which together may be considered as a local computer bus." (emphasis added)

As seen from the above, each node in the Parrish et al. system is simply a standard computer. This places the Parrish et al. system squarely into the "multicomputer" (more than one full computer) category of the Bell reference (see pg. 39, col. 1, paragraph marked 5), which as evidenced from the figure on pg. 37 also places Parrish et al. squarely into the "message-passing" category. Not only that, but the citation on pg. 39, col. 1, paragraph 5 of Bell clearly states: "When data movement is required ... the compiler generates ***messages*** to transfer data to other nodes", further evidencing that such groupings of plural computers inherently are a "message passing" type architecture.

F. That: "Referring to the feature "not on a common bus", the Examiner states that in Figure 2 of the Parrish reference, [sic] one can see that the VME Bus and the VSB Bus are not common to the local memories. From this the Examiner concludes that the memories are not on a common bus. This is simply not so. The fact that there are buses in the Parrish architecture, [sic] is not pertinent. The Interconnect bus 160 is a common bus. Therefore, the local memories are on a common bus, even though there may be further buses that are not common."

This is not found persuasive because applicant's argument appears to be directed to the

rejection of claim 34 as claim 34 recites that the local data memories of the first and second processor elements are not on a common bus, and applicant's argument above references those local memories. Applicant's exact claim language is:

> "the local data memories of the at least first and second processor elements not on a common bus;"

As seen from figure two, Parrish et al. shows "the local data memories (113, IPM, 114, ILM, 133, IPM, 134, ILM) of the at least first (100, NODE A) and second (120, NODE B) processor elements (100, 120) not on a common bus (160). As is clearly seen from fig. 2, memories IPM and ILM (113, 114) of NODE A (100) are on (directly connected to) VME Bus 115 and VSB Bus 116 of NODE A (100). Memories IPM and ILM (133, 134) of NODE B (120) are on (directly connected to) VME Bus 135 and VSB Bus 136. As noted above, Parrish et al. indicates that each of NODE A and NODE B are "industry standard digital computer[s]". Therefore, based upon fig. 2 and this statement, it is clear that busses 115 and 116 of NODE A are not connected in common to busses 135 and 136 of NODE B. I.e., bus 115 of NODE A does not have a cable extending outside the housing of NODE A, entering the housing of NODE B, and attaching to bus 135 of NODE B. Therefore, bus 115 is not "in common" with bus 135 because they are not directly connected. The same reasoning applies to buses 116 and 136, as there is no direct connection between these busses of the different nodes, busses 116 and 136 are not "in common". As the memories (113, 114, 133, 134) of the different nodes (100, 120) are only on (directly connected to) busses 115 and 116 or 135 and 136, the memories of the individual nodes are not on (directly connected to) any common bus.

Stated in another way, in the Parrish et al. system, the memories are on (directly connected to) only busses internal to the nodes and because the nodes are individual computer systems the memories therefore can not be seen as being on any common bus.

Affidavit of Anton Gunzinger

12. Mr. Gunzinger, the sole inventor of the present application, has submitted an affidavit asserting certain material as factual and as showing certain conclusions. As Mr. Gunzinger's

affidavit did not indicate whether it was a 37 CFR § 1.131 or § 1.132 affidavit, and because it attempts to show secondary considerations, it is being treated as a § 1.132 affidavit.

13. Mr. Gunzinger's 1.132 affidavit makes one assertion and two submissions. The single assertion, in paragraph 5, makes an unsubstantiated assertion that there are two different categories of classification for parallel computers. However, paragraph 5 is merely an assertion lacking any factual evidence to support the assertion. As detailed in MPEP § 716.01(c) an affidavit must be supported by factual evidence. Lacking any factual evidence support for paragraph 5, the mere assertion by the inventor (a person who has great interest in the outcome of this case) has no merit.

14. The first submission made in Mr. Gunzinger's 1.132 affidavit occurs in paragraph 6. In paragraph 6 Mr. Gunzinger refers to pg. 640 of Patterson and Hennessy. However, Mr. Gunzinger makes no further reference to pg. 640 of Patterson et al. beyond that it is a widely known standard textbook and includes a chapter on parallel processing. No nexus to the claimed invention, and no statement of what fact is being relied upon from pg. 640 of Patterson et al. is presented by Mr. Gunzinger. Therefore, lacking any explanation as to why pg. 640 is Patterson et al. is cited, paragraph 6 also has no merit. Furthermore, Patterson et al. has been extensively treated in the previous rejections and been found to not support applicants assertions and instead to fully support the Examiner's line of reasoning.

15. The second submission made in Mr. Gunziner's 1.132 affidavit occurs in paragraph 7, where Mr. Gunzinger simply states that attached is the Gordon Bell publication which also has been extensively treated above in the response to applicant's arguments. Again, Mr. Gunzinger makes no attempt at explaining a nexus to the claimed invention, and makes no statement as to what fact is being derived from the Bell publication. Therefore, again lacking any explanation as to why Bell is being cited, paragraph 7 also has no merit. Furthermore the Bell publication has also been extensively treated above, and also found to not support applicant's assertions and instead to fully support the Examiner's line of reasoning.

16. A shortened statutory period for response to this action is set to expire 3 (three) months

and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

17. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (571) 272-4165. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (571) 272-4162. The fax phone number for the USPTO is: (703)872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-2100.

Richard Ellis
December 21, 2005

RICHARD L. ELLIS
PRIMARY EXAMINER